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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/723,563	11/28/2000	U-Ming Ko	TI-29632	5590

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EXAMINER	
WILLIAMS, ALEXANDER O	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 02/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Applicati n No.	Applicant(s)	
	09/723,563	KO, U-MING	
	Examiner	Art Unit	
	Alexander O Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Peri d for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *42-63* is/are pending in the application.

4a) Of the above claim(s) *52-63* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *42-51* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Pri rity under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 09/723563 Attorney's Docket #: TI-29632
Filing Date: 11/28/00;
Applicant: Ko

Examiner: Alexander Williams

Applicant's Amendment filed 11/29/04 to the Amendment/Election of Species of electrostatic discharge device (claims 42-51) filed 7/23/03 has been acknowledged.

This application contains claims 52 to 63 drawn to an invention non-elected without traverse.

Claims 1-41 have been canceled.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 42 to 51 are rejected under 35 U.S.C. § 102(e) as being anticipated by Zhang (U.S. Patent # 4,750,081 A).

Fir example, in claim 42, Zhang (figures 1 to 6) specifically figures 1 and 2 show an integrated circuit having a plurality of I/O modules, comprising: a substrate **(semiconductor substrate under 18)**; a bond pad **18** disposed on said substrate; an electrostatic discharge device **(within the semiconductor substrate)** disposed in the substrate, the electrostatic discharge device being at least partially beneath the bond pad; circuitry (inherit) disposed in said substrate; an I/O buffer **19-22** disposed in the

substrate and connected to the bond pad for providing communication between the bond pad and said circuitry said circuitry positioned substantially adjacent to both the electrostatic discharge and the I/O buffer.

In U.S. Pat. No. 4,750,081, an electrostatic discharge protection circuit is disclosed having diodes located directly beneath the rectangular corners of a wirebond pad. Also, discrete diodes may be formed directly beneath the perimeter or the marginal portion of the pad in a row between the corner diodes, the longitudinal extension of these other diodes being perpendicular to the sides of the pad. The major portion of the pad will thus have no metal layers therebelow, reducing the risk of delamination. Only diodes of a single orientation type are used connecting the metal pad to the substrate by a reverse-biased pn-junction.

ABSTRACT:

An integrated circuit chip having improved static discharge protection comprises a semiconductor substrate with a major surface, a plurality of transistors that are integrated into the surface, patterned conductors that interconnect the transistors and route input signals to the transistors, with the patterned conductors including metal pads for receiving the input signals from an external source; wherein the improvement comprises respective diodes which are integrated into the surface directly beneath the metal pads, and which connect the pads to the substrate and conduct electrostatic charge therebetween. With this structure, no additional chip space is required over that which is used by the transistors which are being protected since the diodes are hidden in the normally unused chip space beneath the pads. Also with this structure, the diodes can be large since the metal pads are inherently large enough to receive a bonding wire; and thus the diodes have a large current-carrying capacity and a small series resistance. Preferably, the metal pads have sharp corners of 90.degree. or less which tend to accumulate any electrostatic charge, and the diodes are disposed beneath the metal pads at these corners. Since the diodes are located where the charge tends to accumulate, they are more effective in dissipating that charge than if they were located elsewhere.

(8) In accordance with the invention, an integrated circuit chip having improved static discharge protection comprises a semiconductor substrate with a major surface, a plurality of

transistors that are integrated into the surface, patterned conductors that interconnect the transistors and route input signals to the transistors, with the patterned conductors including metal pads for receiving the input signals from an external source; wherein the improvement comprises respective diodes which are integrated into the surface directly beneath the metal pads, and which connect the pads to the substrate and conduct electrostatic charge therebetween. With this structure, no additional chip space is required over that which is used by the transistors which are being protected since the diodes are hidden in the normally unused chip space beneath the pads. Also with this structure, the diodes can be large since the metal pads are inherently large enough to receive a bonding wire; and thus the diodes have a large current-carrying capacity and a small series resistance.
Preferably, the metal pads have sharp corners of 90.degree. or less which tend to accumulate any electrostatic charge, and the diodes are disposed beneath the metal pads at these corners. Since the diodes are located where the chargetends to accumulate, they are more effective in dissipating that charge than if they were located elsewhere.

Claims 42 to 51 are rejected under 35 U.S.C. § 102(e) as being anticipated by Schroen et al. (U.S. Patent # 6,303,977 B1).

For example, in claim 42, Schroen et al. (figures 1 to 2B) specifically figure 1 show an integrated circuit **100** having a plurality of I/O modules, comprising: a substrate **104**; a bond pad **118** disposed on said substrate; an electrostatic discharge device **(under 118)** disposed in the substrate, the electrostatic discharge device being at least partially beneath the bond pad; circuitry (inherit) disposed in said substrate; an I/O buffer **113a** disposed in the substrate and connected to the bond pad for providing communication between the bond pad and said circuitry said circuitry positioned substantially adjacent to both the electrostatic discharge and the I/O buffer.

(18) The invention also applies to chips designs with sacrificial metal structures embedded in the dielectric layers close to the sawing lines, and to designs having reinforcing metal structures under the bonding pads. For illustration purposes, an example of the latter design concept is depicted in FIG. 1. Portions 119 of the integrated circuit are positioned under one of the bonding pads; examples include interconnects,

portions of protective structures against electrostatic discharge, precision resistors, capacitors and inductors. For electrical biasing reasons, some parts of the circuit portions may have electrical connections 120 to diffused moats 121 or other connections 122 to the semiconductor substrate. In addition, portions 123 of a reinforcing dummy structure are shown, electrically isolated from the circuit patterns.

Claims 42 to 51 are rejected under 35 U.S.C. § 102(e) as being anticipated by Anh (U.S. Patent # 6,373,109).

For example, in claim 42, Ahn (figures 1 to 8) specifically figures 2 and 3 show an integrated circuit **10** having a plurality of I/O modules , comprising: a substrate **121**; a bond pad **124c** disposed on said substrate; an electrostatic discharge device **(within 121)** disposed in the substrate, the electrostatic discharge device being at least partially beneath the bond pad; circuitry (inherit) disposed in said substrate; an I/O buffer **128** disposed in the substrate and connected to the bond pad for providing communication between the bond pad and said circuitry said circuitry positioned substantially adjacent to both the electrostatic discharge and the I/O buffer.

(6) An impurity layer 127 which electrically connects the impurity layer 126c of the drain-wire contact portion to the impurity layer 126b serving as the drain of the ESD protecting device is formed in the semiconductor substrate 121 under the dummy gate electrode 124c. Further, a silicide layer 128 is formed on the gate electrodes 124a, 124b, the dummy gate electrode 124c and the impurity layers 126a, 126b, 126c. The dummy gate electrode 124c of a polysilicone layer, instead of the silicide layer, as well as the gate electrodes 124a, 124b are formed on a portion of the drain of the ESD protecting device, thereby maintaining high drain resistance. Also, the semiconductor device according to the present invention decreases wire contact resistance by forming the silicide layer 128 on the impurity layers at the drain-wire contact portion.

(7) FIG. 3 is a cross-sectional view illustrating a semiconductor device according to a second embodiment of the present invention. The difference between the semiconductor devices according to the first and second embodiments of the present invention is in that in the first embodiment the dummy gate electrode 124c is formed on the drain of the ESD protecting device, while in the second embodiment a dummy gate electrode

124d is formed on a drain and a source of an ESD protecting device, and in the second embodiment of the present invention an impurity layer 127 is formed in a semiconductor substrate 121 under the dummy gate electrode 124d. Accordingly, those elements which are the same as the elements in the semiconductor device according to the first embodiment of the present invention are given the same reference numbers.

Response

Applicant's arguments filed 11/29/04 have been fully considered, but are moot in view of the new grounds of rejections detailed above.

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/786,784,357,723,777,691,203,723,725,360,401,205-207,382,377,409,173,362,384,635,355,107,111,173,174,356,358,363,546,547,409,350,372,213,360,603 361/56,111,220,91	11/4/02 11/20/03 9/15/04 1/28/05
Other Documentation: foreign patents and literature in 257/786,784,357,723,777,691,203,723,725,360,401,205-207,382,377,409,173,362,384,635,355,107,111,173,174,356,358,363,546,547,409,350,372,213,360,603 361/56,111,220,91	11/4/02 11/20/03 9/15/04 1/28/05
Electronic data base(s): U.S. Patents EAST	11/4/02 11/20/03 9/15/04 1/28/05

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AOW
1/29/05

Primary Patent Examiner
Alexander O. Williams